

## **Renesas Technology Completes Design of CPU Core for Next-Generation Microcontrollers, and introduces details of ‘RX Family’**

*—The new MCUs will be built on a 90-nm flash process and achieve the world’s top-class performance and code efficiency among CISC devices –*

TOKYO, November 8, 2007 — Renesas Technology Corp. today announced that it has completed the design of an innovative new CISC<sup>(1)</sup> (Complex Instruction Set Computer) CPU architecture that will deliver unmatched capabilities in code efficiency, processing performance, and power consumption for a future generation of Renesas’ CISC microcontrollers (MCUs). Products based on the new architecture will be branded as the ‘RX’ family.

The first family utilizing the Renesas’ eXtreme MCU core, RX is destined to bring excellent performance and versatility to many end systems in the coming years. When RX devices, built around 16-bit and 32-bit versions of the new CPU, become available, Renesas expects that they will accelerate the expansion of its MCU business and support the company’s vision of a ubiquitous networked society.

Today’s embedded systems involve more complex designs that require higher performance, multiple functions, and the use of advanced technology. As a result, system complexity and program sizes increase, and MCUs must run faster and more efficiently in order to execute large application programs in real-time.

As the world’s top MCU supplier<sup>(2)</sup>, Renesas has a broad product portfolio of MCUs, including the M16C, H8S, R32C and H8SX families that address 16- and 32-bit markets. The strong global demand for these popular devices, coupled with forecasts for continued market growth, especially in the 32-bit market, has encouraged Renesas to invest the substantial R&D resources necessary to make the new architecture a reality.

Important characteristics achieved in the new RX architecture, which fully satisfy the objectives announced in May 2007, are as follows:

1. Maximum operating frequency: 200MHz
2. Processing performance (MIPS/MHz): 1.25 MIPS/MHz (Dhrystone v2.1 benchmark)
3. High code efficiency<sup>(3)</sup>: 30% reduction in object-code size compared to existing products
4. Low power consumption: 0.03 mA/MHz
5. Compatibility and scalability with existing products

The new RX architecture with powerful CISC instructions will provide these enhanced capabilities while at the same time unifying Renesas’ existing CISC architectures into a single platform. The new platform will be compatible with existing CISC products, allowing customers to preserve their investments. The first of the enhanced MCUs are expected to become available in the second quarter of 2009. The primary target markets include office automation, digital consumer electronics and industrial systems.

## Additional details of key characteristics of RX architecture

- **Fast, high-performance CPU** — The new architecture provides high-speed operation (200MHz) while at the same time processes more instructions per clock cycle: 1.25MIPS/MHz, as measured in the Dhrystone v2.1 benchmark.

The new CPU is based on a Harvard Architecture, which provides separate address and data paths, allowing the execution of instructions and data access in single cycle. This single-cycle capability was also tested and verified using field-proven Renesas MCUs. To ensure the highest performance possible, Renesas has performed extensive design and testing work on the architecture. As a result, the new architecture is fully optimized with the efficient use of registers, instructions and address modes. Moreover, it has sixteen 32-bit general-purpose registers, which allow the CPU to process both data and addresses in all available registers.

- **On-chip floating point unit** — To enable highly sophisticated real-time control and multimedia applications, the RX CPU incorporates critical functions such as a multiply, divide, and multiply/accumulate. It also implements an IEEE754-compliant 32-bit single-precision floating-point processing unit (FPU) for handling multiple data types. The FPU reduces the calculation time for data processing tasks, the number of cycles needed for mathematical calculations, and the response time for any event occurrence, providing enhanced real-time performance.

- **Highly efficient use of code** — The RX CPU core has 4GB of address space and supports twelve types of address modes including Register Indirect with Index and Post Increment . The new CPU core supports byte-unit variable-length execution instructions that range from 1 to 9 bytes. It assigns 1- or 2-byte instructions to the most frequently used functions. All these enhancements compile application code in smaller program memory space, reducing overall system cost. Renesas expects that the new core will be thirty percent more code efficient compared to existing Renesas devices.

- **Low power consumption** — The newly developed 90-nm process that will be used to build the MCU with the RX architecture is a low-power, low-current-leakage technology. The improvements in logic and circuit designs help the new architecture to achieve 0.03mA/MHz or less power consumption at active mode when the CPU is running at full speed.

- **Compatibility and scalability** — To provide customers with seamless upgrade paths for higher performance MCUs or other compatible devices, Renesas plans to offer a complete suite of development tools for all devices with the RX architecture. The new toolchain is expected to simplify the migration of system designs and application code, so customers will need less time to complete new product development. The new toolchain including a C compiler will ensure the reuse of code, protecting the customers' investments made in the H8 and M16C families.

For more information about the new CISC architecture, visit [www.america.renesas.com/newmcucore](http://www.america.renesas.com/newmcucore)

### About Renesas Technology Corp.

Renesas Technology Corp. is one of the world's leading semiconductor system solutions providers for mobile, automotive and PC/AV (Audio Visual) markets and the world's No.1 supplier of microcontrollers. It is also a leading provider of LCD Driver ICs, Smart Card microcontrollers, RF-ICs, High Power Amplifiers, Mixed Signal ICs, System-on-Chip (SoC), System-in-Package (SiP) and more. Established in 2003 as a joint venture between Hitachi, Ltd. (TSE:6501, NYSE:HIT) and Mitsubishi Electric Corporation (TSE:6503), Renesas Technology achieved consolidated revenue of 953billion JPY in FY2006 (end of March 2007). Renesas Technology is based in Tokyo, Japan and has a global network of manufacturing, design and sales operations in around 20 countries with about 26,500 employees worldwide. For further information, please visit <http://www.renesas.com>

**Notes:**

1. CISC stands for “Complex Instruction Set Computer.” This type of CPU architecture boosts control processing performance and code efficiency by using complex instructions. CISC contrasts with RISC (Reduced Instruction Set Computer), a type of CPU architecture designed to increase data processing efficiency through the use of a simplified instruction set and high-speed technology.
2. Source: Garter Dataquest (March 2007) "2006 Worldwide Microcontroller Vendor Revenue" GJ07168
3. Code efficiency: an index of program compactness. The higher the object-code efficiency, the less memory is needed to store programs.

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**Specifications for new Renesas Technology "RX: CPU core**

<b>Item</b>	<b>RX CPU Specifications</b>
CPU core	"RX" CISC type
Maximum operating frequency	200MHz
Register	32 bits x 16
Basic instructions	87 <ul style="list-style-type: none"><li>• Variable-length instruction format ( 1 to 9 bytes)</li><li>• Three operand format supporting</li></ul>
Endian mode	<ul style="list-style-type: none"><li>• Little-endian instructions</li><li>• Data by big or little endian</li></ul>
Address space	4GB
Addressing modes	12 types (Shortening register relative, Register indirect with post-increment, Register indirect with pre-decrement, Index register indirect, etc )
Floating point unit	IEEE754-compliant, single-precision floating-point unit (Supporting add, subtract, compare, multiply, divide. etc.)
Multiplier unit	High-speed multiplier unit (32-bit x 32-bit -> 64-bit)
Divider unit	High-speed divider unit (32-bit / 32-bit -> 64-bit)
Multiply-and-accumulate unit	High-speed multiply-and-accumulate unit (32-bit x 32-bit + 80-bit -> 80-bit)
MIPS performance (target)	Over 1.25 MIPS/MHz (Dhrystone 2.1)
Power consumption (target)	0.03 mA/MHz or less

